

EXM32

Baseboard Design Guide

Revision 1.0

2008-09-11

Copying of this document, and giving it to others and the use or communication of the contents thereof, are forbidden without express authority. Offenders are liable to the payment of damages. All rights are reserved in the event of the grant of a patent or the registration of a utility model or design.

Document change history

<i>Date</i>	<i>Version</i>	<i>Document change description</i>
2008-09-11	10	Release version

Table of Contents

DOCUMENT CHANGE HISTORY	2
TABLE OF CONTENTS	3
1 INTRODUCTION	4
1.1 PURPOSE	FEHLER! TEXTMARKE NICHT DEFINIERT.
1.2 DEFINITIONS, ACRONYMS AND ABBREVIATIONS	4
1.3 REFERENCES	5
2 OVERVIEW	6
2.1 CONCEPT	6
2.2 EXM32 PIN DEFINITION ON BASEBOARD	6
3 MECHANICAL RECOMMENDATIONS	7
3.1 EXM32 MODULE FOOTPRINT	7
3.1.1 <i>Dimensions on Baseboard</i>	7
3.1.2 <i>"Pin-1" Mark</i>	8
3.1.3 <i>Contact Pad Geometry & Mechanical Tolerances</i>	8
3.1.4 <i>Alignment Holes</i>	8
3.1.5 <i>Solder mask</i>	9
3.1.6 <i>Keep Out Area</i>	9
3.1.7 <i>Power Pads</i>	9
3.1.8 <i>Stacking of modules</i>	10
3.2 MODULE MOUNTING ISSUES	10
3.2.1 <i>Nuts</i>	10
3.2.2 <i>Screws</i>	10
3.2.3 <i>Thread Locking</i>	10
3.3 EXM32 SYSTEM ASSEMBLY - CONNECTOR ISSUES	11
3.3.1 <i>Dust and particles</i>	11
3.3.2 <i>Assembly</i>	11
4 SUMMARY OF DOS & DON'T'S FOR EXM32 MB DESIGN	12
5 EXM32 BUS SPECIFICATION	13
5.1 CONNECTOR X1 (CPU BUS, COMPACT FLASH, SPI, AC'97/I ² S, PCI-E).....	13
5.2 CONNECTOR X2 (INTERFACES)	14
5.3 SIGNAL DESCRIPTION	15
5.3.1 <i>Connector X1</i>	15
5.3.2 <i>Connector X2</i>	19
6 FUNCTIONAL UNITS	26
6.1 USB 2.0 INTERFACE.....	26
6.2 FIREWIRE (IEEE1394A (DATA STROBE)) INTERFACE.....	27
6.3 DUAL CAN INTERFACE	28
6.4 VGA GRAPHIC ON BASEBOARD	29
6.5 LCD 1 INTERFACE ON BASEBOARD	30
6.6 LCD 2 /GPIO INTERFACE ON BASEBOARD.....	32
6.7 DIGITAL AUDIO (AC97, I2S) INTERFACE ON BASEBOARD.....	34
6.8 MMC/SD/SDIO INTERFACE ON BASEBOARD.....	36
6.9 COMPACT FLASH INTERFACE ON BASEBOARD	37
6.10 ETHERNET INTERFACE ON BASEBOARD	39
6.11 EXTERNAL UART ON BASEBOARD.....	FEHLER! TEXTMARKE NICHT DEFINIERT.
6.12 SYSTEM PLL ON BASEBOARD.....	FEHLER! TEXTMARKE NICHT DEFINIERT.
6.13 SYSTEM RESET ON BASEBOARD.....	FEHLER! TEXTMARKE NICHT DEFINIERT.
6.14 BOARD ID.....	FEHLER! TEXTMARKE NICHT DEFINIERT.
6.15 POWER SUPPLY	40
6.16 ESD.....	40
6.17 EMC	FEHLER! TEXTMARKE NICHT DEFINIERT.
7 SW RELATED DESIGN ISSUES	FEHLER! TEXTMARKE NICHT DEFINIERT.
7.1 CPU & I/O ADDRESS DEFINITION	FEHLER! TEXTMARKE NICHT DEFINIERT.
7.2 RESET CONFIGURATION	FEHLER! TEXTMARKE NICHT DEFINIERT.
7.3 INTERRUPT STRUCTURE	FEHLER! TEXTMARKE NICHT DEFINIERT.

1 Introduction

1.1 Objective

This document is the technical design guide for baseboards compatible to the MSC EXM32 embedded controller module standard. This document is a reference for dimension, pin out and signal/interface definitions of EXM32 compatible baseboards.

1.2 Target Audience

This specification is intended for hardware engineers who design EXM32 modules or baseboards. Experience in designing 32-bit controller boards and multi-layer, printed circuit boards is assumed.

1.3 Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided "as is" and is subject to change without notice.

1.4 Trademarks

All used product names, logos or trademarks are property of their respective owners.

1.5 Technical Support

Before contacting the Technical Support of the EXM32 Users & Manufacturers Group, please consult the respective pages on the web site (www.exm32.org) for the latest documentation.

If the information provided there does not solve your problem, you will find the contact details of our Technical Support there.

1.6 Definitions, Acronyms and Abbreviations

EXM32	Embedded eXtensible Module for 32-bit Processors
SPI	Serial Protocol Interface
USB	Universal Serial Bus
CAN	Controller Area Network
CRT	Cathode Ray Tube
I ² C	Inter-IC
I ² S	Inter-IC Sound
CF	Compact Flash
ETH	Ethernet
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
TFT	Thin Film Transistor
STN	Super Twisted Nematic
MMC	MultiMedia Card
SD-Card	Secure Digital Memory Card
SDIO	Secure Digital I/O Card
AC'97	Audio Codec '97

1.7 References

USB Specification 1.1

CAN Specification Version 2.0

CompactFlash Specification Revision 1.4

I²C-BUS Specification Version 2.1

PCI Express www.intel.com/technology/pciexpress/ & www.pcisig.com/home

2 Overview

2.1 Concept

The EXM32 CPU module family is targeted to automotive and industrial control applications. Customized systems can be developed easily and fast using a standard EXM32 CPU module as a system building block and a customer-specific baseboard which provides power supply, application specific circuits and interface connectors.

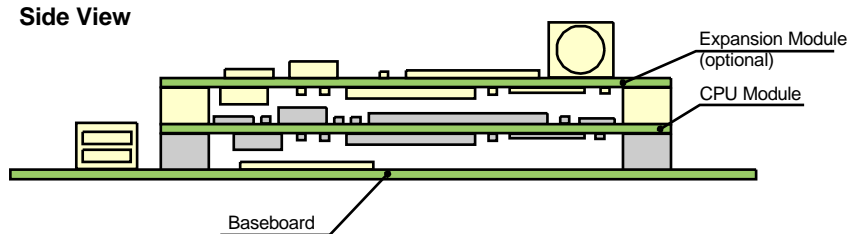


Figure 1 EXM32 System Example

The EXM32 connector system uses highly reliable elastomeric contact elements in a robust shell. In contrast to a conventional plug/socket connector assembly the EXM32 connector consists only of one mechanical connector element.

The connection between two modules is established by compressing the contact elements in between two module boards with matching contact pads.

The connector technology allows for stacking of several modules.

2.2 EXM32 Pin Definition on Baseboard

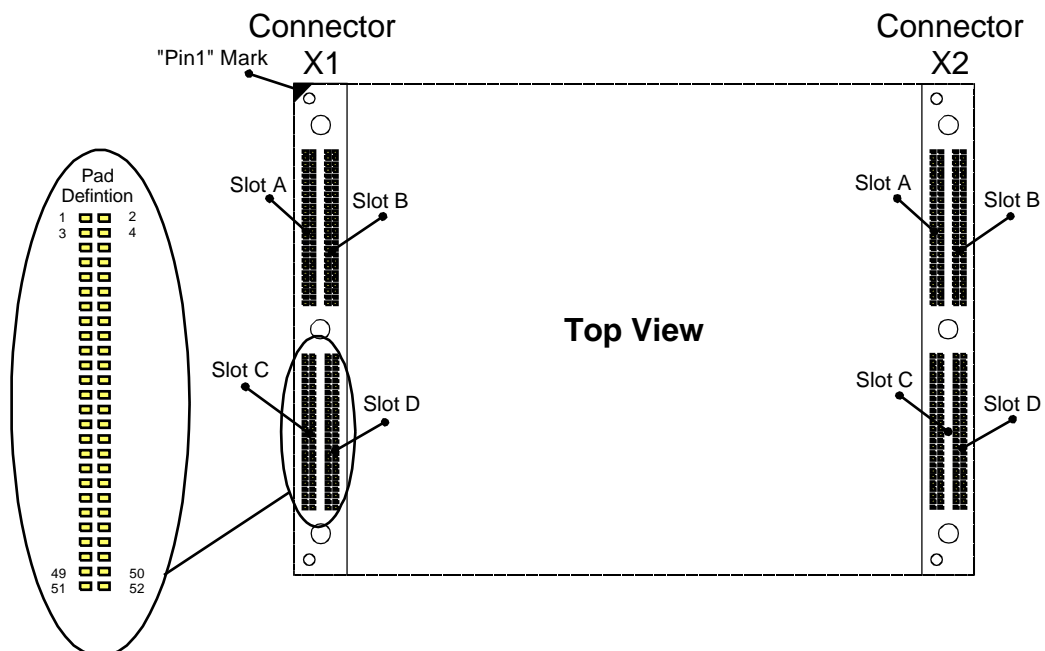


Figure 2 EXM32 Module Pin Definition on Baseboard

3 Mechanical Recommendations

3.1 EXM32 Module Footprint

3.1.1 Dimensions on Baseboard

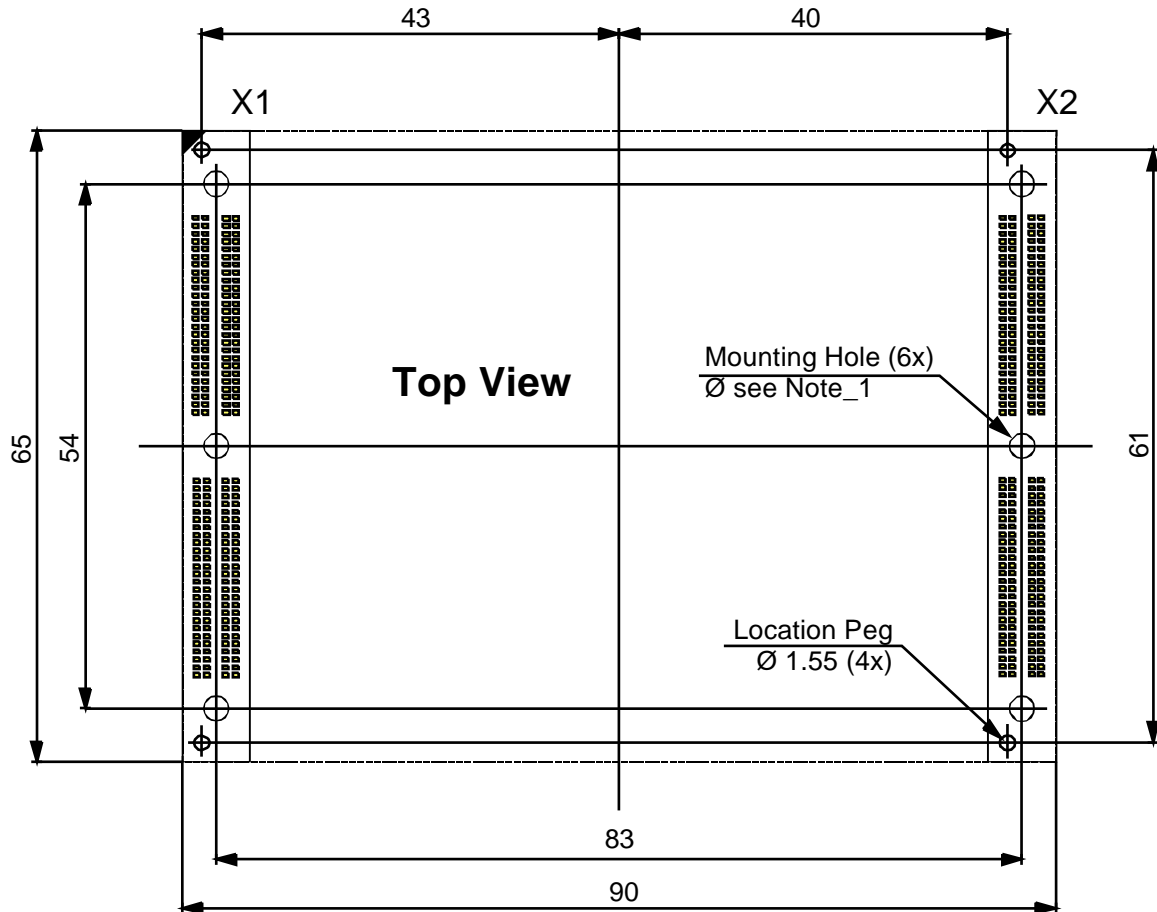


Figure 3 EXM32 Module Footprint Dimensions on Baseboard

Note:

The diameter of the mounting holes depends on the fastening method used. We recommend using threaded inserts soldered to the board. The diameter is 4.8 -0/+0.2mm plated.

3.1.2 “Pin-1” Mark

The baseboard should have a “pin 1” mark corresponding with the “pin 1” mark of the EXM32 modules (refer to Figure 2).

Incorrect mounting of the system can damage the CPU and Extension modules.

3.1.3 Contact Pad Geometry & Mechanical Tolerances

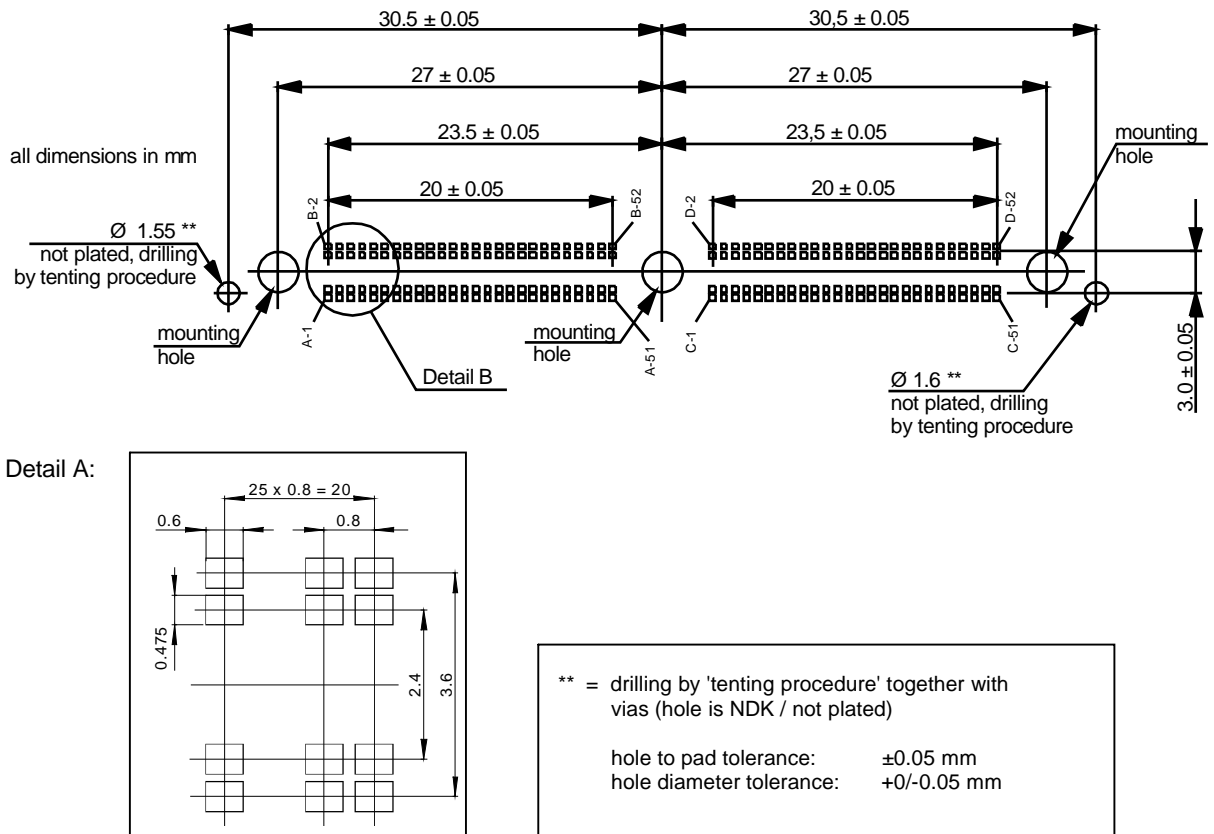


Figure 4 EXM32 Connector Pad Layout

3.1.4 Alignment Holes

The alignment hole's diameter is defined to 1.55 +0/-0.05 mm. It is recommended to enlarge one hole per connector to 1.6 +0/-0.05 mm to allow for some thermal expansion.

The base board should have only two alignment holes per connector, thus providing correct orientation of the upper EXM32 module.

3.1.5 Solder mask

The complete EXM32 Connector area must be kept free of solder mask to assure proper contact:

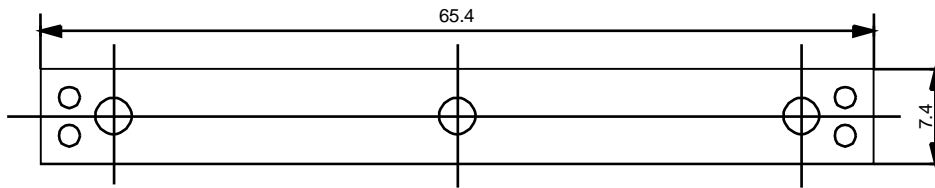


Figure 5 EXM32 Connector solder mask

3.1.6 Keep Out Area

Do not place vias or route on the connector-layer in the hatched areas:

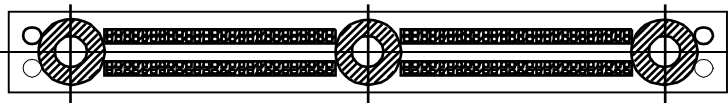


Figure 6 EXM32 Connector keep out area

Keep out area around mounting holes (top and bottom side):

- 7.25 mm Ø

Keep out area around contact pads:

- pad size + 0,2 mm hole

Inner layers can be used without limitations.

3.1.7 Power Pads

Power contact pads of the same supply are connected together to build a continuous area over all pad locations. This provides the maximum current capacity.



Example:

The following pads must be connected to power-areas:

Connector X1 - A:

- GND Pad 29 to 52 (2x 12 pads)

Connector X1 - C:

- VCC3V3 Pad 1 to 12, 13, 15 17, 19, 21, 32 (1x 12, 1x 6 pads)
- VCC3V3STB Pad 14, 16, 18, 20, 22, 24 (1x 6 pads)
- VCC5V0 Pad 26, 28, 30, 32, 34, 36 (1x 6 pads)

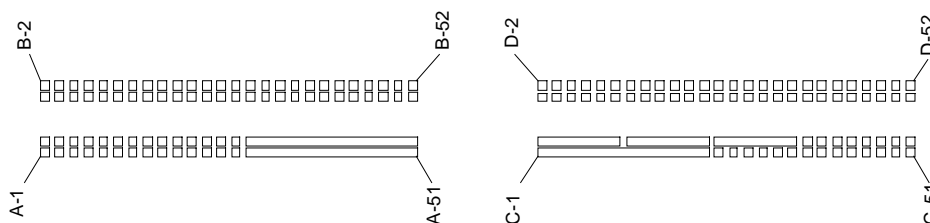


Figure 7 EXM32 Connector X1 - footprint with power plane areas

3.1.8 Stacking of modules

A baseboard (= bottom PCB in a module stack) should have only two alignment holes per EXM32 Connector so a module can't be mounted in the wrong direction.

When multiple modules are stacked, the modules in the middle of the stack must have four center pins for every EXM32 Connector location to allow stacking of the upper module:

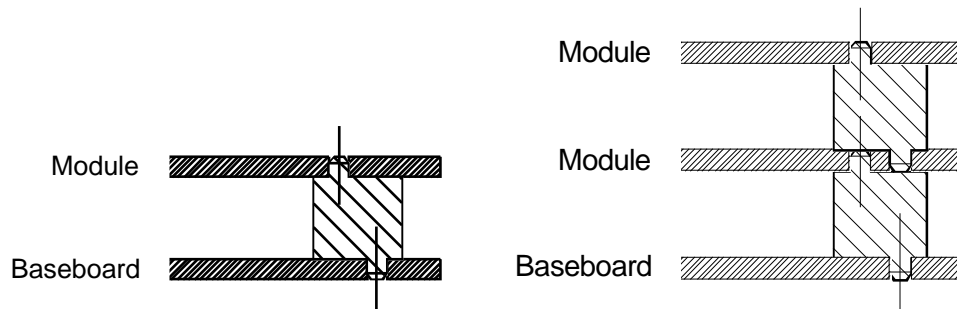


Figure 8 EXM32 module stacking

3.2 Module Mounting Issues

3.2.1 Nuts

There are several methods of mounting an EXM32 module on a baseboard. The most frequently used method is to fasten the modules with soldered threaded inserts and TORX-screws.

3.2.2 Screws

M2.5 Torx screws (DIN 7985 - ISO 7045):

- 12mm screws for two-module-stacks
- 20mm screws for three-module-stacks

3.2.3 Thread Locking

When the system shall be used in a heavy duty application, it is recommended to apply thread locking like Loctite® or Tuflok® coated screws.

3.3 EXM32 System Assembly - Connector Issues

3.3.1 Dust and particles

For a reliable connection the PCB's contact pads have to be clean and free from dust or other particles. Therefore after soldering the PCBs either need to be washed or the contact zone be cleaned separately. Residues of fluxing chemicals may create major problems.

The contact zone must be absolutely free from any solder, because solder causes long-term contact failures or may prevent the full compression of the elastomeric connector.

Cleaning recommendations:

- Remove dust and particles with the adhesive area of "Post-it" type notes or by compressed air.
- Clean the contacts using isopropanol / isopropyl alcohol (medical grade), only, and a soft brush if required.

3.3.2 Assembly

First insert the EXM32 connectors location pins into the alignment holes of the lower PCB / baseboard without force:

- Stack all modules onto the baseboard in the correct order (see manuals) without using force or laterally dislocating them.
- Gently hold down the modules pressing down perpendicularly with one hand.
- Insert the 6 screws into the mounting holes.
- Fasten the M2,5 screws using a torque wrench at 30 Ncm torque.

4 Summary of Dos & Don'ts for EXM32 Baseboard Design

What to bear in mind during the layout design phase:

- Make sure the entire "landing zone" of the Elastomeric Connector is completely free of solder mask - not just single pads (this is the most common mistake in all EXM32 baseboards designs !).
It is also recommended to specifically inform the PCB manufacturer that this is intended and not a bug in your design !
- The alignment holes absolutely **MUST** be produced using the "Tenting" procedure – meaning that the holes are drilled in the same process step as the vias without getting plated by masking them with a resist "lid" (very important) !!! Tenting is a standard procedure and no reason for surcharges.
- Neighbouring pads of the same signal or voltage (e.g. VCC, GND) should be connected by completely closing the gap between the pads with signal tracks (see 3.1.7).
- When the module is fastened using soldered threaded inserts it is important that the holes have got a min. diameter of 4.8 mm instead of the 4.2mm diameter used if you actually **PRESS** them in.
- The tolerances for the alignment holes should be communicated very clearly to the PCB manufacturer so that they cannot be forgotten and in order to eliminate excuses.
- Do **NOT** route tracks between the pads of the connector in the contact zone.
- The contact pads have to be erased from the paste mask so they do not get covered with solder paste !!! It is recommended to specifically communicate to contractors / production staff that the contact pads absolutely must not come in contact with solder and to check the paste mask before starting a production run.
- The board **MUST** be NiAu plated (standard plating – no special procedures) in order to guarantee long-term reliability.
- Minimum board thickness is 1,6mm using FR-4 material. Thinner boards must use a stiffener under the connector area in order to maintain the required pressure on the contact zone.

The schematics of the EXM32-Motherboard-LITE are available to members of the EXM32 consortium.

5 EXM32 Bus Specification

5.1 Connector X1

X1 - A			
Pin	Signal	Pin	Signal
1	IDE_IORDY	2	CF_SCKSEL
3	IDE_CS0#	4	CF_CE1#
5	IDE_CS1#	6	CF_CE2#
7	CF0_PWEN	8	CF_IORD# IDE_DIOR#
9	CF1_PWEN	10	CF_IOWR# IDE_DIOW#
11	CF_INPACK#	12	CF_POE#
13	CF0_RESET	14	CF_PWE#
15	CF1_RESET	16	CF_WAIT#
17	SPI_SS0#	18	CF_IOIS16#
19	SPI_SS1#	20	CF_PREG#
21	reserved, don't use	22	CF0_RDY_IRQ#
23	SPI_SCK	24	CF1_RDY_IRQ#
25	SPI_MOSI	26	CF0_CD#
27	SPI_MISO	28	CF1_CD#
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND

X1 - B			
Pin	Signal	Pin	Signal
1	D00	2	D01
3	D02	4	D03
5	D04	6	D05
7	D06	8	D07
9	D08	10	D09
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	D16	18	D17
19	D18	20	D19
21	D20	22	D21
23	D22	24	D23
25	D24	26	D25
27	D26	28	D27
29	D28	30	D29
31	D30	32	D31
33	BE0#	34	BE1#
35	BE2#	36	BE3#
37	IRQ_EXT1#	38	reserved, don't use
39	IRQ_EXT0#	40	CSA#
41	IRQ_MB2#	42	CSB#
43	IRQ_MB1#	44	BS#
45	IRQ_MB0#	46	OE#
47	CLK_GND	48	WE#
49	CLKOUT	50	R/W#
51	CLK_GND	52	RDY

X1 - C			
Pin	Signal	Pin	Signal
1	VCC3V3	2	VCC3V3
3	VCC3V3	4	VCC3V3
5	VCC3V3	6	VCC3V3
7	VCC3V3	8	VCC3V3
9	VCC3V3	10	VCC3V3
11	VCC3V3	12	VCC3V3
13	VCC3V3	14	VCC3V3STB
15	VCC3V3	16	VCC3V3STB
17	VCC3V3	18	VCC3V3STB
19	VCC3V3	20	VCC3V3STB
21	VCC3V3	22	VCC3V3STB
23	VCC3V3	24	VCC3V3STB
25	VBAT	26	VCC5V0
27	reserved, don't use	28	VCC5V0
29	PWROFF/SUSPEND	30	VCC5V0
31	SLEEP#	32	VCC5V0
33	WAKEUP	34	VCC5V0
35	PWRFLT#	36	VCC5V0
37	RESET_IN#	38	ETH_ACTLED#
39	RESET_OUT#	40	ETH_LNKLED#
41	AC_RESET#	42	AC'97_SDIN1
43	AC'97_SYNC/ I ² S0_LRCLK	44	AC'97_SDIN0 / I ² S0_SCK
45	I ² S1_LRCLK	46	I ² S1_SCK
47	AC_GND	48	AC'97_SDOOUT / I ² S0_SDIO
49	AC'97_BCLK / I ² S_MCLK	50	I ² S1_SDIO
51	AC_GND	52	reserved, don't use

X1 - D			
Pin	Signal	Pin	Signal
1	A00	2	A01
3	A02	4	A03
5	A04	6	A05
7	A06	8	A07
9	A08	10	A09
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	A16	18	A17
19	A18	20	A19
21	A20	22	A21
23	A22	24	A23
25	A24	26	A25
27	DREQ0#	28	DREQ1#
29	DRAK0#	30	DRAK1#
31	DACK0#	32	DACK1#
33	PCIE_WAKE#	34	PCIE_PRSENT#
35	PCIE_PERST#	36	PCIE_REFCLK+
37	PCIE_PWRON	38	PCIE_REFCLK-
39	PCIE_GND	40	PCIE_GND
41	PCIE_GND	42	PCIE_PET0+
43	PCIE_GND	44	PCIE_PET0-
45	PCIE_GND	46	PCIE_GND
47	PCIE_GND	48	PCIE_PER0+
49	PCIE_GND	50	PCIE_PER0-
51	PCIE_GND	52	PCIE_GND

5.2 Connector X2

X2 - A			
Pin	Signal	Pin	Signal
1	FW_GND	2	FW_CPS
3	FW_TP0A+	4	MLB_CLK
5	FW_TP0A-	6	MLB_SI
7	FW_GND	8	MLB_SO
9	FW_TP0B+	10	MLB_DI
11	FW_TP0B-	12	MLB_DO
13	FW_GND	14	JTAG_TDO
15	FW_TP1A+	16	JTAG_TDI
17	FW_TP1A-	18	JTAG_TCK
19	FW_GND	20	JTAG_TMS
21	FW_TP1B+	22	JTAG_TRST#
23	FW_TP1B-	24	CAN0_EN
25	FW_GND	26	CAN1_RX
27	SATA_TX+	28	CAN0_ERR#
29	SATA_TX-	30	CAN1_TX
31	SATA_GND	32	CAN0_STB#
33	SATA_RX+	34	CAN1_EN
35	SATA_RX-	36	CAN0_RX
37	SATA_GND	38	CAN1_ERR#
39	USB_GND	40	CAN0_TX
41	USB0_D+	42	CAN1_STB#
43	USB0_D-	44	USB0_ID
45	USB_GND	46	USB0_VBUS
47	USB1_D+	48	USB0_PWEN
49	USB1_D-	50	USB1_PWEN
51	USB_GND	52	USB_OC#

X2 - B			
Pin	Signal	Pin	Signal
1	DA_GND	2	DA_GND
3	DA0_SPDIF	4	DA1_SPDIF
5	DA_GND	6	DA_GND
7	DA0_MCLK	8	DA1_MCLK
9	DA_GND	10	DA_GND
11	DA0_SCLK	12	DA1_SCLK
13	DA0_LRCLK	14	DA1_LRCLK
15	DA0_SDIN0	16	DA1_SDOOUT0
17	DA0_SDIN1	18	DA1_SDOOUT1
19	DA0_SDIN2	20	DA1_SDOOUT2
21	DA_MUTE	22	DA_ERR
23	DV_GND	24	DV_GND
25	DV0_CLK	26	DV1_CLK
27	DV_GND	28	DV_GND
29	DV0_AV#	30	DV1_AV#
31	DV0_HSYNC / DV0_SYNC	32	DV1_HSYNC / DV1_SYNC
33	DV0_VSYNC / DV0_DVALID	34	DV1_VSYNC / DV1_DVALID
35	DV_GND	36	DV_GND
37	DV0_D0	38	DV1_D0
39	DV0_D1	40	DV1_D1
41	DV0_D2	42	DV1_D2
43	DV0_D3	44	DV1_D3
45	DV0_D4	46	DV1_D4
47	DV0_D5	48	DV1_D5
49	DV0_D6	50	DV1_D6
51	DV0_D7	52	DV1_D7

X2 - C			
Pin	Signal	Pin	Signal
1	LCD_D00 (B0)	2	I2C0_SDA
3	LCD_D01 (B1)	4	I2C0_SCL
5	LCD_D02 (B2)	6	I2C1_SDA
7	LCD_D03 (B3)	8	I2C1_SCL
9	LCD_D04 (B4)	10	ETG_GND
11	LCD_D05 (B5)	12	ETH_TXD1+
13	LCD_D06 (G0)	14	ETH_TXD1-
15	LCD_D07 (G1)	16	ETH_GND
17	LCD_D08 (G2)	18	ETH_TXD0+
19	LCD_D09 (G3)	20	ETH_TXD0-
21	LCD_D10 (G4)	22	ETH_GND
23	LCD_D11 (G5)	24	ETH_RXD0+
25	LCD_D12 (R0)	26	ETH_RXD0-
27	LCD_D13 (R1)	28	ETH_GND
29	LCD_D14 (R2)	30	ETH_RXD1+
31	LCD_D15 (R3)	32	ETH_RXD1-
33	LCD_D16 (R4)	34	VGA_GND
35	LCD_D17 (R5)	36	VGA_R
37	LCD_VDON	38	VGA_GND
39	LCD_M_DE	40	VGA_G
41	LCD_VCON	42	VGA_GND
43	LCD_HSYNC	44	VGA_B
45	LCD_VSYNC	46	VGA_GND
47	LCD_DON	48	VGA_H
49	LCD_SHFCLK	50	VGA_V
51	LCD_BLON	52	VGA_GND

X2 - D					
Pin	Signal		Pin	Signal	
	GPIO	LCD			GPIO
1	GP_IN7	LCD2_D00	2	n.c.	LCD2_VDON
3	GP_IN6	LCD2_D01	4	n.c.	LCD2_M_DE
5	GP_IN5	LCD2_D02	6	n.c.	LCD2_VCON
7	GP_IN4	LCD2_D03	8	n.c.	LCD2_HSYNC
9	GP_IN3	LCD2_D04	10	n.c.	LCD2_VSYNC
11	GP_IN2	LCD2_D05	12	n.c.	LCD2_DON
13	GP_IN1	LCD2_D06	14	n.c.	LCD2_SHFCLK
15	GP_IN0	LCD2_D07	16	n.c.	LCD2_BLON
17	GP_OUT7	LCD2_D08	18		SDIO_WP
19	GP_OUT6	LCD2_D09	20		SDIO_CLK
21	GP_OUT5	LCD2_D10	22		SDIO_CD#
23	GP_OUT4	LCD2_D11	24		SDIO_CMD
25	GP_OUT3	LCD2_D12	26		SDIO_DAT0
27	GP_OUT2	LCD2_D13	28		SDIO_DAT1/IRQ#
29	GP_OUT1	LCD2_D14	30		SDIO_DAT2/RW
31	GP_OUT0	LCD2_D15	32		SDIO_DAT3
33	LCD2_EN		34		CPUID0_IN
35	MODULE_DETECT		36		CPUID1_IN
37	COM0_TXD		38		FR_TXD
39	COM0_RXD		40		FR_RXD
41	COM0_RTS#		42		FR_TXEN#
43	COM0_CTS#		44		FR_RXEN#
45	COM1_TXD		46		FR_BGE
47	COM1_RXD		48		FR_EN
49	COM1_RTS#		50		FR_STB#
51	COM1_CTS#		52		FR_ERR#

5.3 Signal Description

Please note that all pins "reserved, don't use" must not be used for general purpose hardware. They may be used in specific combinations of CPU modules and baseboards.

All Signals are 3,3V LVTTTL signals unless specified otherwise.

5.3.1 Connector X1

N.C.	not connected
I.C.	internal connected - not to be used by customer
GND	logic ground
VCC3V3	3.3 VDC \pm 5% main power supply
VCC3V3STB	3.3 VDC standby voltage (e.g. for self-refreshing SDRAM, CPU in sleep mode)
VCC5V0	5.0 VDC \pm 10% optional power supply
VBAT	battery voltage (e.g. for real-time clock, battery is on EXM32 Baseboard)

5.3.1.1 SPI Bus Interface

Up to two SPI (Serial Peripheral Interface) bus channels may be provided on EXM32 CPU modules.

SPI_SCK	Serial Clock output signal
SPI_MOSI	Master Output / Slave Input signal
SPI_MISO	Master Input / Slave Output signal
SPI_SS<1:0>#	Slave Select signals, active low

5.3.1.2 ATA/ATAPI Interface

ATA/ATAPI interface is provided on EXM32 CPU modules.

Note: The ATA and the CompactFlash interface share some signals.

IDE_CS<1:0>#	Chip select signals from host, used to select the Command Block or Control Block registers. When DACK# is asserted, CS0# and CS1# shall be negated and transfers shall be 16 bits wide.
IDE_DIOR#	DIOR# is the strobe signal used by the host to read device registers or the Data port. Data is transferred on the negation of this signal.
IDE_DIOW#	DIOW# is the strobe signal used by the host to write device registers or the Data port. Data is transferred on the negation of this signal.
IDE_IORDY	IORDY is negated to extend the host transfer cycle of any host register access (read or write) when the device is not ready to respond to a data transfer request. If the device requires that the host transfer cycle time be extended for PIO modes 3 and above, the device shall use IORDY. Hosts that use PIO modes 3 and above shall support IORDY.

5.3.1.3 CompactFlash Interface

The CompactFlash interface supports both "Memory Mode" and "I/O Mode". Address and data lines are connected the CPU bus.

CF<1:0>_CD#	These Card Detect pins are connected to GND on the Compact Flash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
CF_SCKSEL	Allows to multiplex between 2 CF-Slots (0: Slot0; 1: Slot1), glue logic is required, is an output of the EXM32 CPU Module.
CF_CE<2:1>#	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the Odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1# and CE2 # allows 8 bit hosts to access all data on D0-D7.
CF_IORD#	This signal is not used in PC Card Memory Mode. in "PC Card I/O Mode" this signal is an I/O Read strobe generated by the host. It gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface, active low.
CF_IOWR#	This signal is not used in PC Card Memory Mode. in "PC Card I/O Mode" the I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (raising edge), active low.
CF_POE#	Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers, active low.
CF<1:0>_RDY_IRQ#	in PC Card Memory Mode: In Memory Mode this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card or CF+ Card has been powered up with +RESET continuously disconnected or asserted. in PC Card I/O Mode: The signal is IREQ# . After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
CF<1:0>_RESET	When the pin is high, this signal resets the CompactFlash Storage Card or CF+ Card. The CompactFlash Storage Card or CF+ Card is reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+ Card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
CF<1:0>_PWEN	When the pin is set high, the power supply for Compact Flash socket is enabled.
CF_PWE#	in PC Card Memory Mode: This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers only.
CF_WAIT#	The WAIT# signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
CF_IOIS16#	in PC Card Memory Mode: Used as Write Protect signal. The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. in PC Card I/O Mode: When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation, the signal indicates if the selected I/O is a 16 Bit Port (IOIS16#). A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed data port.
CF_PREG#	in PC Card Memory Mode:

This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.

in PC Card I/O Mode:

The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.

5.3.1.4 CPU Bus

D<31:00>	CPU Data bus lines
A<25:00>	CPU Address bus lines
BE<3:0>#	Byte Enable signals for write cycles only, BE0# indicates the least significant byte, active low
CSA#, CSB#	Chip Select signals for external devices, active low
OE#	Output Enable signal (read strobe), active low
WE#	Write Enable signal (write strobe), active low
R/W#	Read/Write signal for direction control of Data Bus buffers, output from CPU Module, write cycle = low
RDY	Ready signal from peripheral, indicates that a transfer is complete, active high
BS#	Bus Start signal, indicates the start of a bus cycle, active low
RESET_IN#	CPU Module Reset Input, active low
RESET_OUT#	This output is the system reset generated from the CPU Module to reset external devices, active low
CLKOUT	System Clock, generated by the CPU Module
CLK_GND	Clock GND, used for shielding / controlled impedance
IRQ_EXT<1:0>#	Interrupt Request from Extension Modules, active low, IRQ_EXT0# has highest priority
IRQ_MB<2:0>#	Interrupt Request from Baseboard, active low, IRQ_MB0# has highest priority
DREQ<1:0>#	DMA Request Inputs are used by external devices to indicate whether they need service from the CPU modules DMA controller, active low.
DRAK<1:0>#	DMA Request Acknowledge outputs, notifies acceptance of DMA transfer request to external device which has output DREQ#; active low.
DACK<1:0>#	DMA Acknowledge outputs, notification Strobe output to external device which has output DREQ#; active low.
PWRFLT#	Module input, indicates that the primary power supply voltage of the baseboard is dropping below the operating voltage range. This signal can be used to save a limited amount of data in a non-volatile memory before the CPU shuts down or to enter sleep mode using VCC BAT.
SLEEP#	Sleep output, this signal is used to indicate the CPUs sleep mode to external devices, active low.
PWROFF/SUSPEND	Power Off/Suspend output, this signal is used to shutdown supply voltages, only VSTBY and VBAT may be available, active high.
WAKEUP	Wakeup CPU from Sleep mode, input for CPU module, active high.

5.3.1.5 Audio Codec Interface AC'97 and I²S Interface

Serial data can be received from and transmitted to an AC'97 or I²S codec on the baseboard. All signals are LV-TTL level signals. Up to two digital sound channels may be provided from EXM32 CPU modules:

	I²S mode:	AC'97 mode:
AC_RESET#	Codec Reset, active low	Codec Reset, active low
AC'97_BCLK / I²S_MCLK	Master Clock (only master mode)	Serial Data Clock (Bit Clock)
Channel 0:		
AC'97_SYNC / I²S0_LRCLK	Left/Right Channel Select (Word Select)	Frame Sync
AC'97_SDIN0 / I²S0_SCK Codec)	Serial Bit Clock	Serial Data In (Primary
AC'97_SDIN1 Codec)	no function	Serial Data In (Secondary
AC'97_SDOUT / I²S0_SDIO	Serial Data Out	Serial Data Out
I²S1_SDIO	Serial Data In	
Channel 1:		
I²S1_LRCLK	Left/Right Channel Select (Word Select)	no function
I²S1_SCK	Serial Bit Clock	no function
AC_GND	Audio Codec Ground for shielding purposes	

5.3.1.6 PCI Express x1 Master Interface

Contact pads for one PCIE connection lane is provided in the EXM32 CPU modules specification. The PCIE signals are intended to serve as:

PCIE_PET0+	Transmitter Signal positive (signal available only on bottom pad layout)
PCIE_PET0-	Transmitter Signal negative (signal available only on bottom pad layout)
PCIE_PER0+	Receiver Signal positive (signal available only on bottom pad layout)
PCIE_PER0-	Receiver Signal negative (signal available only on bottom pad layout)
PCIE_REFCLK+	Reference Clock Signal positive (signal available only on bottom pad layout)
PCIE_REFCLK-	Reference Clock Signal negative (signal available only on bottom pad layout)
PCIE_PRSENT#	present signal (active low)
PCIE_WAKE#	wake-up signal (active low)
PCIE_PERST#	reset signal (active low)
PCIE_PWRON	power on signal (active high)
PCIE_GND	PCIE GND for shielding / controlled impedance

5.3.2 Connector X2

5.3.2.1 IEEE1394 (Firewire™)

Up to two IEEE1394 ports are provided on EXM32 CPU modules.

FW_TP<1:0>A+	Twisted-Pair A Differential-Signals pos. (signal available only on bottom pad layout)
FW_TP<1:0>A-	Twisted-Pair A Differential-Signals neg. (signal available only on bottom pad layout)
FW_TP<1:0>B+	Twisted-Pair B Differential-Signals pos. (signal available only on bottom pad layout)
FW_TP<1:0>B-	Twisted-Pair B Differential-Signals neg. (signal available only on bottom pad layout)
FW_CPS	Cable Power Status
FW_GND	IEEE1394 GND for shielding / controlled impedance

5.3.2.2 Serial ATA

One Serial ATA port is provided on EXM32 CPU modules.

SATA_TX+	Transmitter Signal positive
SATA_TX-	Transmitter Signal negative
SATA_RX+	Receiver Signal positive
SATA_RX-	Receiver Signal negative
SATA_GND	SATA GND for shielding / controlled impedance

5.3.2.3 USB

Note: All pull-up resistors are integrated on the EXM32 CPU module.

USB0_D+, USB0_D-	Serial Data Pair for USB Port0, USB0_D+ - positive signal, USB0_D- - negative signal
USB1_D+, USB1_D-	Serial Data Pair for USB Port1, USB1_D+ - positive signal, USB1_D- - negative signal
USB0_ID	USB OTG Configuration ID, High= peripheral, Low=host
USB0_VBUS	USB Supply Voltage, also used for OTG Session Request Protocol
USB<1:0>_PWEN	USB Bus Power Enable signal, active high, enables the USB ports +5V supply
USB_OC#	Over Current Detect Signal for the USB +5V power line from baseboard, common for two USB ports, active low
USB_GND	USB GND for shielding / controlled impedance

5.3.2.4 JTAG Interface

JTAG signals are used only for boundary scan and PLD programming.

JTAG_TDO	Data return path from the module on top or the local JTAG chain to the bottom module / baseboard.
JTAG_TDI_IN	Data-path from the bottom module/baseboard to the local JTAG-chain and the debug connector
JTAG_TDI_OUT	Data-path from the local JTAG-chain TDO output to the next module's TDI input
JTAG_TCK	Functions as the serial clock input pin stipulated in the JTAG standard (IEEE standard 1149.1).
JTAG_TMS	Mode Select input - Changing this signal determines the significance of data input via the TDI pin. Its protocol conforms to the JTAG standard.
JTAG_TRST#	JTAG Reset signal is received asynchronously with TCK signal. Asserting this signal resets the JTAG interface circuit.

5.3.2.5 MOST Media Local Bus Interface

One Media Local Bus is provided on EXM32 CPU modules. All signals are LV-TTL level signals.

	5-pin mode (default):	3-pin mode:
MLB_CLK	clock input	clock input (MLBCLK)
MLB_SI	signal information input	no function
MLB_SO	signal information output	signal information in/out (MLBSIG)
MLB_DI	data input	no function
MLB_DO	data output	data in/out (MLBDAT)

5.3.2.6 CAN

Up to two CAN Bus interfaces are provided on EXM32 CPU modules. All signals are LV-TTL level signals. External CAN transceivers are required to convert the LV-TTL signals to the physical CAN interface.

CAN<1:0>_TX	transmit data
CAN<1:0>_RX	receive data
CAN<1:0>_ERR#	bus error flag, active low
CAN<1:0>_EN	transceiver enable, active high
CAN<1:0>_STB#	transceiver standby, active low

5.3.2.7 Digital Audio Interface

Up to two digital audio interfaces provided on the EXM32 CPU modules. All signals are LV-TTL level signals.

Digital Audio Channel 0:

DA0_SPDIF	Digital Audio signal (IEC 60958)
DA0_MCLK	Master Clock
DA0_SCLK	Serial Bit Clock
DA0_LRCLK	Left/Right Channel Select (Word Select)
DA0_SDIN0	Serial Data Input 0
DA0_SDIN1	Serial Data Input 1
DA0_SDIN2	Serial Data Input 2

Digital Audio Channel 1:

DA1_SPDIF	Digital Audio signal (IEC 60958)
DA1_MCLK	Master Clock
DA1_SCLK	Serial Bit Clock
DA1_LRCLK	Left/Right Channel Select (Word Select)
DA1_SDOUT0	Serial Data Output 0, contains channel 1 (Left) and channel 2 (Right) information
DA1_SDOUT1	Serial Data Output 1, contains channel 3 (Left Surround) and channel 4 (Right Surround) information
DA1_SDOUT2	Serial Data Output 2, contains channel 5 (Center) and channel 6 (Low Frequency Effect) information
DA_ERR	Audio Error signal
DA_MUTE	Audio Mute signal
DA_GND	Digital Audio Ground for shielding purposes

5.3.2.8 Digital Video Interface

Two digital video interfaces may be provided on EXM32 CPU modules. All signals are LV-TTL level signals.

Digital Video Channel 0:

DV0_CLK	Video Clock signal
DV0_D<7:0>	Channel 0 data lines
DV0_AV#	Available signal, active low
DV0_HSYNC	Horizontal Sync signal, high active
DV0_SYNC	Sync signal, indicates the start of packet, high active
DV0_VSYNC	Vertical Sync signal, high active
DV0_DVALID	Data Valid signal, indicates if data is valid for reading or writing, high active

Digital Video Channel 1:

DV1_CLK	Video Clock signal
DV1_D<7:0>	Channel 1 data lines
DV1_AV#	Available signal, active low
DV1_HSYNC	Horizontal Sync signal, high active
DV1_SYNC	Sync signal, indicates the start of packet, high active
DV1_VSYNC	Vertical Sync signal, high active
DV1_DVALID	Data Valid signal, indicates if data is valid for reading or writing, high active
DV_GND	Digital Video Ground for shielding purposes

5.3.2.9 Primary LCD Port

All signals are LV-TTL level signals.

LCD_D<17:00>	Data for LCD panel	
LCD_HSYNC	LCD Horizontal Sync signal	
LCD_VSYNC	LCD Vertical Sync signal	
LCD_SHFCLK	LCD Pixel Clock	
LCD_VDON	enables Supply Voltage for Display Logic	
LCD_VCON	enables Power Inverter Voltage	
LCD_DON	Display On signal for STN displays	
LCD_BLON	enables Backlight	
	in case of STN Display:	in case of TFT Display:
LDC_M_DE	AC Bias signal (M)	LCD Data Enable (DE)

5.3.2.10 I²C Interface

Up to two I²C channels may be provided on EXM32 CPU modules. All signals are LV-TTL level signals.

I2C0_SDA, I2C0_SCL	Serial Data & Clock Input/Output and signal, used to connect the CPU modules on board I ² C units
I2C1_SDA, I2C1_SCL	Serial Data & Clock Input/Output signal, used to connect the CPU modules on board I ² C units

5.3.2.11 Ethernet (1000Mbit)

The signal termination is integrated on the EXM32 CPU Module. The EXM32 Ethernet Interface is designed for use with Ethernet Magnetics.

ETH_TXD0+	Analog Twisted Pair - Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission.
ETH_TXD0-	
ETH_RXD0+	Analog Twisted Pair - Ethernet Receive Differential Pair. These pins receive the serial bit stream from the Ethernet Magnetics.
ETH_RXD0-	
ETH_TXD1+	Analog Twisted Pair - 2 nd Ethernet Transmit Differential Pair for Gigabit Ethernet. These pins transmit the serial bit stream for transmission.
ETH_TXD1-	
ETH_RXD1+	Analog Twisted Pair - 2 nd Ethernet Receive Differential Pair. These pins receive the serial bit stream from the Ethernet Magnetics.
ETH_RXD1-	
ETH_GND	Ethernet GND for shielding / controlled impedance
ETH_ACTLED#	The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
ETH_LNKLED#	The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.

All LED signals pull external LEDs with max. 5 mA to GND.

5.3.2.12 CRT

A standard analogue CRT interface may be provided on EXM32 CPU modules. The 75 Ohm termination resistors are integrated on the EXM32 CPU module.

VGA_R	Red analogue video output signal for CRT displays
VGA_G	Green analogue video output signal for CRT displays
VGA_B	Blue analogue video output signal for CRT displays
VGA_H	Horizontal sync signal: This output supplies the horizontal synchronization pulse
VGA_V	Vertical sync signal: This output supplies the vertical synchronization pulse
VGA_GND	VGA Ground

5.3.2.13 GPIO / Secondary LCD Port

The use of GPIO signals is specific for every EXM32 CPU module, please refer to the dedicated CPU module specification.

All signals are LV-TTL level signals.

Up to 16 I/O signals may be provided by an EXM32 CPU module. These signal pins can alternatively be used as secondary LCD data signals with the signal LCD2_EN indicating the mode:

LCD2_EN when high, the signal indicates that the port is used as 2nd LCD Port :
 high = LCD on GPIO pins
 low = GPIO (default)

LCD mode:

LCD2_D<15:00> Data for LCD panel
LCD2_HSYNC LCD Horizontal Sync signal
LDC2_VSYNC LCD Vertical Sync signal
LCD2_SHFCLK LCD Pixel Clock
LCD2_VDON enables Supply Voltage for Display Logic
LCD2_VCON enables Power Inverter Voltage
LCD2_DON Display On signal for STN displays
LCD2_BLON enables Backlight

	in case of STN Display:	in case of TFT Display:
LDC2_M_DE	AC Bias signal (M)	LCD Data Enable (DE)

GPIO mode:

GP_IN<7:0> General Purpose Input signals for EXM32 CPU module
GP_OUT<7:0> General Purpose Output signals for EXM32 CPU module

Note: The LDC2 Control signals do not have defined levels in GPIO mode.

5.3.2.14 MultiMedia Card / Secure Digital Memory Card/Secure Digital I/O Card

A MultiMedia / Secure Digital Memory / Secure Digital Input/Output Card interface may be provided. All signals are LV-TTL level signals.

SDIO_DAT0 Bidirectional data line 0 (4-bit and 1-bit mode)
SDIO_DAT1/IRQ# Bidirectional data line 1 (4-bit mode), interrupt signal (1-bit mode, only SDIO Card, low active)
SDIO_DAT2/RW Bidirectional data line 2 (4-bit mode), read wait signal (1-bit mode, only SDIO Card, optional)
SDIO_DAT3 Bidirectional data line 3 (4-bit mode)
SDIO_CLK Host to card clock signal
SDIO_CMD Bidirectional command / response signal
SDIO_WP Write protect, active high
SDIO_CD# Card detect, active low

5.3.2.15 Serial Ports

Signals for up to two serial communication interfaces are provided. All signals are LV-TTL level signals. External drivers are required to convert the LV-TTL signals to the desired physical interface like RS232, RS422, RS485.

COM0_TXD	transmit data
COM0_RXD	receive data
COM0_CTS#	handshake signal which notifies the UART that the modem is ready to receive data
COM0_RTS#	handshake signal which notifies the modem that the UART is ready to receive data
COM1_TXD	transmit data
COM1_RXD	receive data
COM1_CTS#	handshake signal which notifies the UART that the modem is ready to receive data
COM1_RTS#	handshake signal which notifies the modem that the UART is ready to receive data

5.3.2.16 FlexRay

A FlexRay interface is provided on EXM32 CPU modules. All signals are LV-TTL level signals. An external transceiver is required to convert the LV-TTL signals to the desired physical interface.

FR_TXD	transmit data
FR_RXD	receive data
FR_TXEN#	transmitter enable, active low
FR_RXEN#	receive data enable, active low
FR_BGE	bus guardian enable
FR_EN	transceiver enable, active high
FR_STB#	transceiver standby, active low
FR_ERR#	bus error flag, active low

5.3.2.17 MISC

MODULE_DETECT	An EXM32 Baseboard can detect if an EXM32 CPU Module is mounted on top, this feature is used for automatic JTAG chain configuration: The EXM32 CPU module provides a VCC3V3 level, the baseboard reads the pin. In case of absence of a CPU Moduzle, the JTAG chain may be closed locally on the baseboard.
CPUID<1:0>	An EXM32 baseboard has the ID value '00'.

6 Functional Units

6.1 USB 2.0 Interface

The EXM32 system module connector offers a two channel USB-Interface on its X2 connector. The USB interface provides USB host functionality on its two channels. Channel 0 can also be configured as a USB-OTG interface if this feature is provided by the EXM32 CPU module. Refer to the according CPU Module datasheet for details.

To provide USB host functionality an external USB power switch (U1401) has to be provided on the baseboard to supply a USB device on the VBUS line. The over current detection of the USB power switch is connected to the EXM-CPU module. If an over current detection occurs an interrupt will be released on the CPU module. The USB data lines are available as a differential pair on the EXM connector and can be connected directly to the USB connector. They have to be routed on the EXM baseboard as a differential pair also. The USB connectors on the baseboard must be type A receptacles when used as a USB host. When USB channel 0 is used as a on-the-go (OTG) controller a type AB receptacle has to be used.

As shown in the example schematic, ESD protection for the external data lines has to be added to the design. The USB ID signal has to be left open when the channel 0 is used as a host controller. If used as a device, connect directly to the ID pin of the AB receptacle.

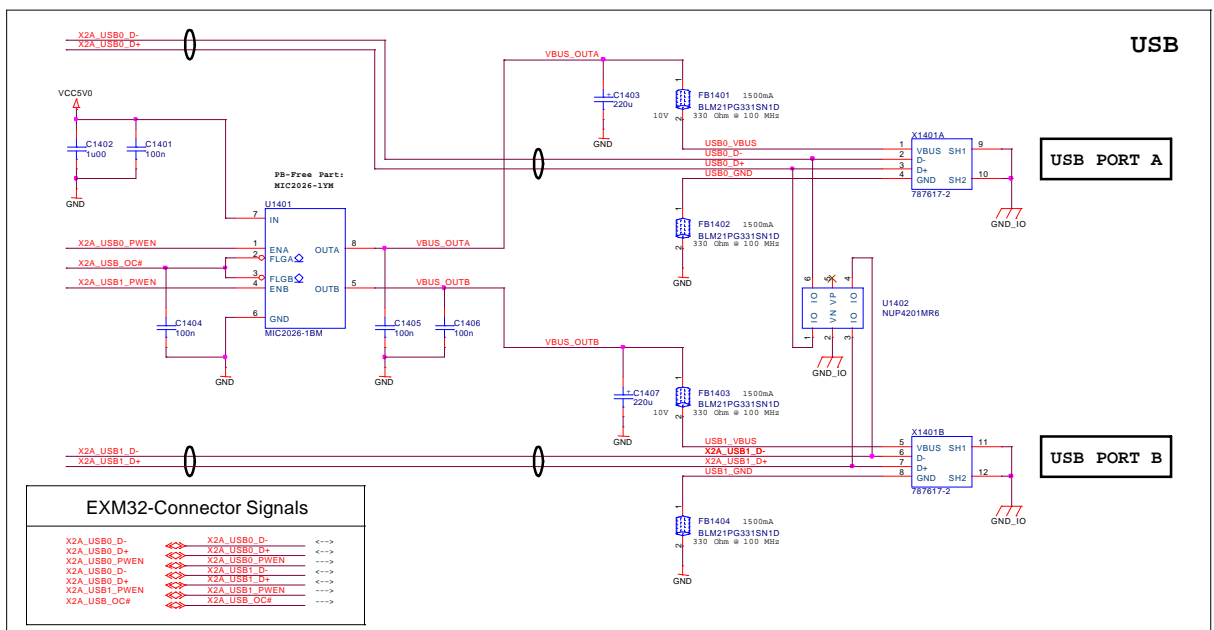


Figure 9 USB example schematic on an EXM32 baseboard

6.2 Firewire (IEEE1394a (Data Strobe)) Interface

A two channel Firewire IEEE1394a (Data Strobe) interface is available on the EXM32 connector X2. The differential pair data lines can be directly connected to the Firewire connector. In accordance to the IEEE1394a specification a 4-pin or a 6-pin connector can be mounted on the baseboard.

The data lines must be routed as differentials pairs on the baseboard. CPS needs to be connected through a series resistor to the Firewire connector on the baseboard as shown in the example below. The CPS voltage may range from 8 to 40 VDC. When using a 4-pin connector CPS is not available. In this case CPS should be connected to ground via a 1KOhm resistor. It is recommended to connect ESD protection diodes to the external differential data lines to avoid damage to the CPU module. The example schematic shows a simple two channel connection for IEEE1394a with ESD protection on the baseboard with 6-pin connectors.

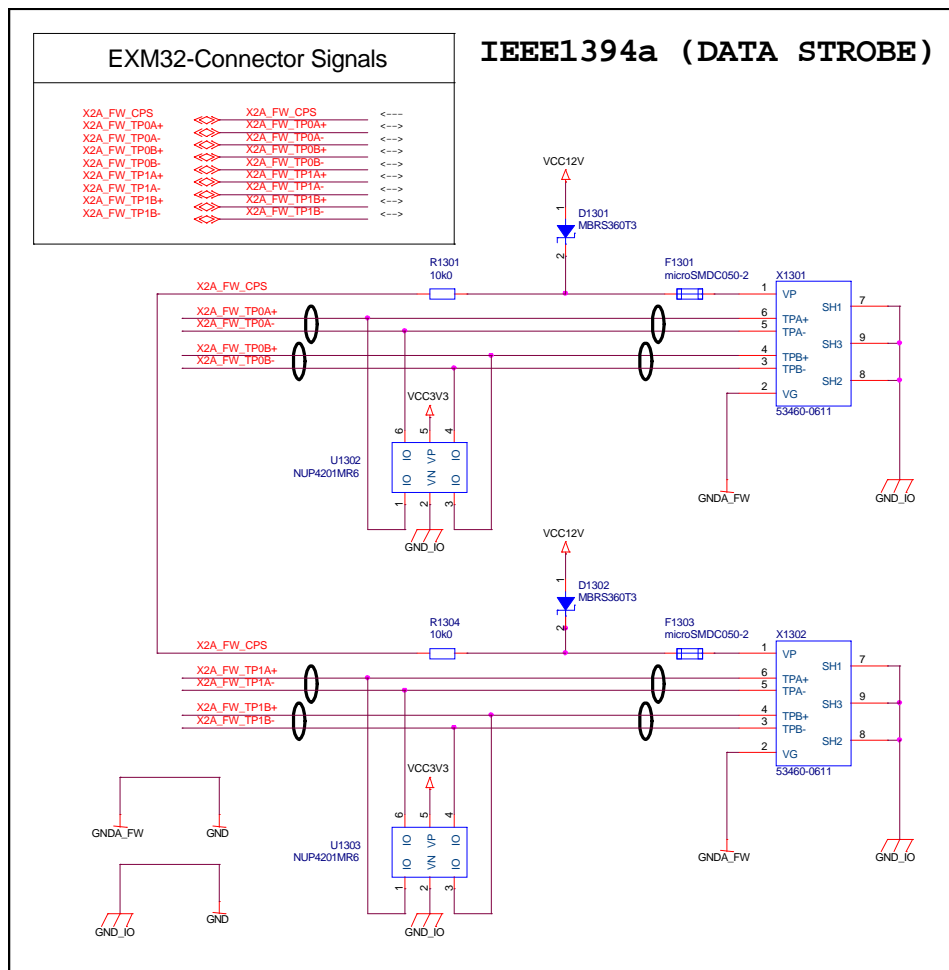


Figure 10 example schematic of an IEEE1394a circuit

Refer to the according CPU-Module datasheet for details.

6.3 Dual CAN Interface

Please note that not every EXM32 module has got a CAN controller populated. In many cases this is an assembly option. The example schematic shows just the connection for one CAN port. The circuit for the second channel is identical. RX and TX must be connected to an external CAN transceiver e.g. like the TJA1040 from NXP.

The signal STB#, available on the EXM connector, can be used to set the CAN transceiver into sleep mode. Depending on the type of CAN transceiver used the low-voltage signals might have 5 volt levels – requiring a level translator as the EXM32 module uses 3,3V levels. The actual design depends very much on customer requirements and more or less any CAN-transceiver may be used as long as the voltage levels to/from the module are LVTTTL. Please refer to the CAN specification for further details.

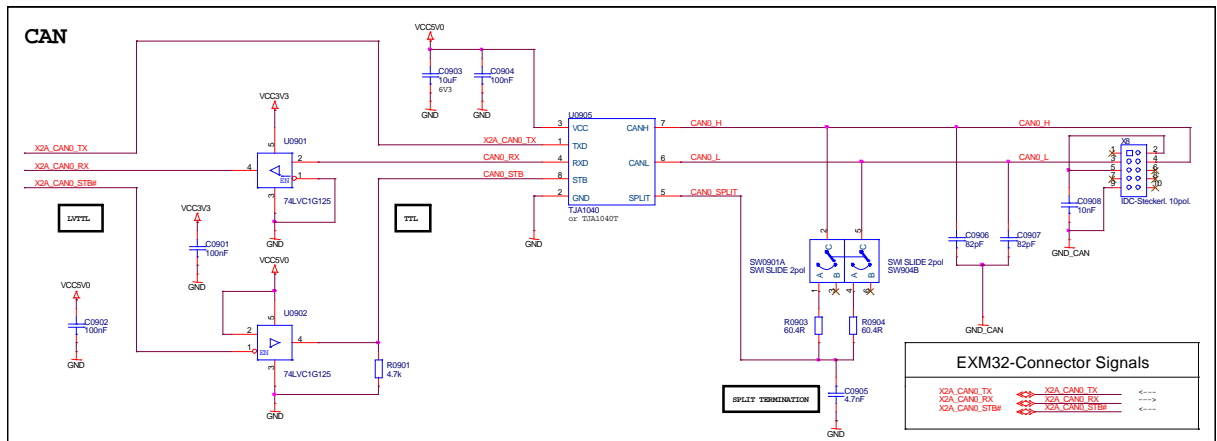


Figure 11 example schematic of a CAN circuit on baseboard

Refer to the according CPU module datasheet for details.

6.4 VGA Graphic on Baseboard

If the EXM-CPU module provides analogue VGA graphic the VGA interface is available on the EXM connector X2. The VGA interface can directly connected to the VGA connector. This is in general a 15 pin SUB-D female connector.

ESD protection has to provided on the baseboard as shown in the example schematic.

A dedicated IC2 bus is provided on the EXM connector (DDC_SDA, DDC_SCL) to read out the displays EPROM.

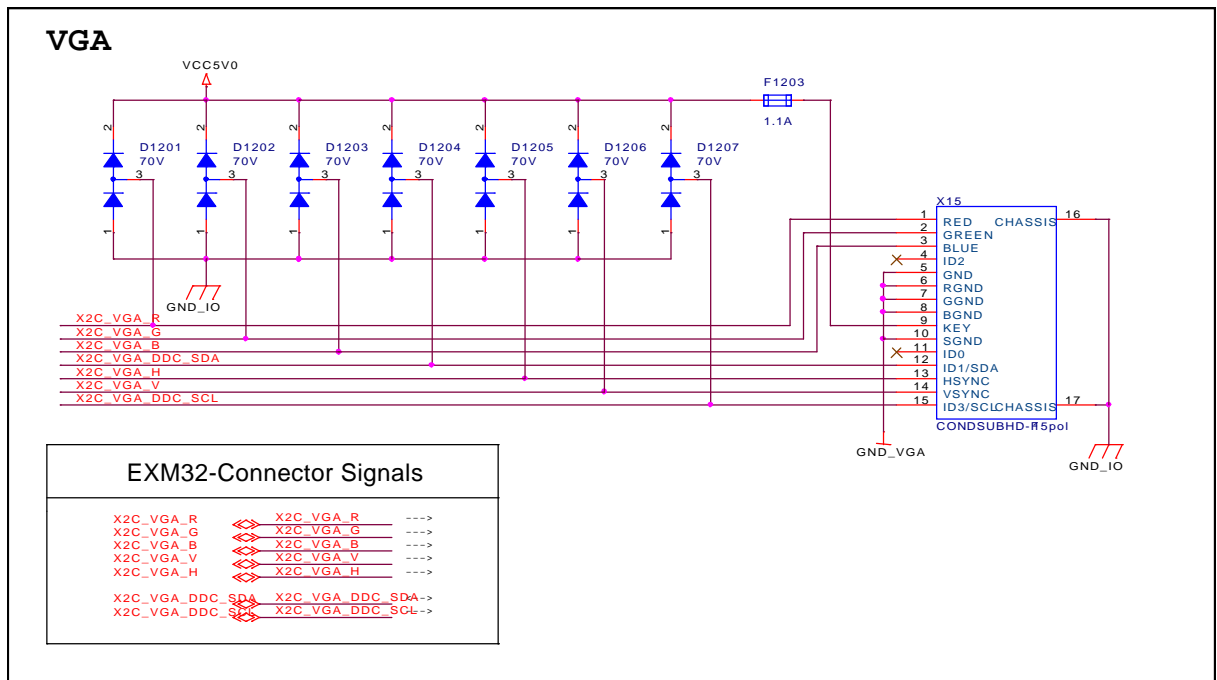


Figure 12 example schematic of a VGA circuit on baseboard

Refer to the according CPU module datasheet for details.

6.5 LCD 1 Interface on Baseboard

The LCD 1 interface at the EXM32 connector allows to connect a 6/8-Bit STN or 12/18- TFT display directly to the EXM-CPU module. The display power control signals are used to control the power up sequence of a STN or TFT display. The supply voltage of a can be 5 or 12V. The signal LCD1_VDON can be used to to enable the logic power with a transistor circuit that is designed to meet the requirements of the used display. The signal LCD1_VCON and LCD1_BLON are used to enable the backlight of a display via a transistor circuit.

The signals LCD_VMODE and LCD_HMODE can be used to mirror the display in vertical or horizontal direction by logic, as shown in the example schematic via jumper or it can be set to a fixed level.

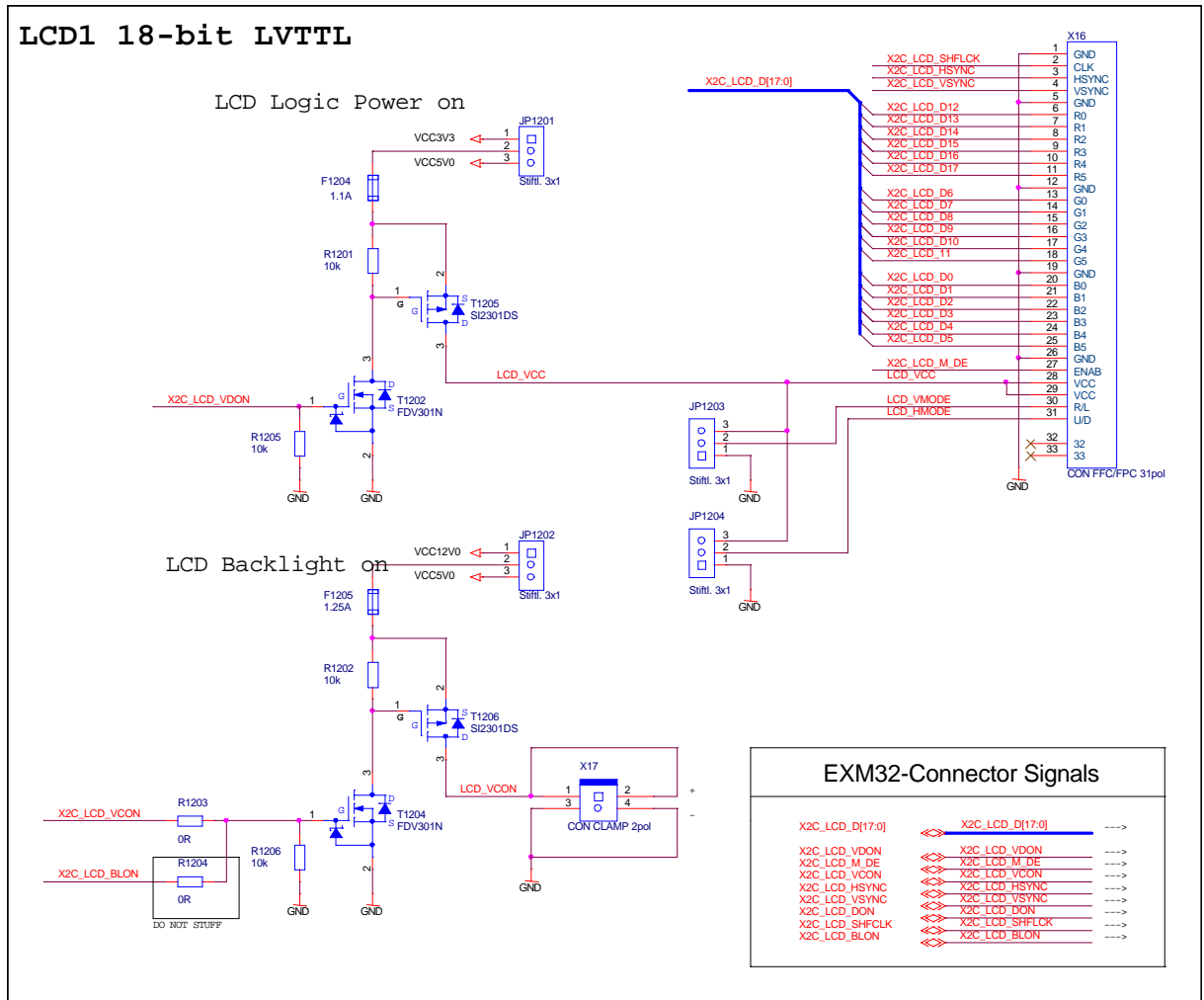


Figure 13 example schematic of an 18-Bit LCD1 Circuit on baseboard

LCD-Interface and EMI Issues:

Please note that the digital LCD interface is one of the most common obstacles when it comes to passing EMI standards. It must be a top design priority to keep the LCD cable and the traces on the board as short as absolutely possible. A 30cm TTL-LCD cable is potentially a major problem.

In order to overcome those problems we recommend to place series resistors in all LCD signals close to the module and to use those resistors to dampen the high-frequency components of the digital signals.

When using buffers to drive the LCD-signals the power supply of those buffers must be filtered very effectively (e.g. using Murata NFE... type filters) and again place series resistors on the output of the buffers. Common values range from 22Ohms to 100Ohms depending on the cable length and pixel frequency.

If possible LVDS signaling should be used, however it's essential to filter the power supply for the transmitter and receivers very carefully.

Filtering is also needed for the digital power supply of the display which may act as an antenna radiating everything which is on the local 3,3V or 5V power plane.

SW Issues:

To achieve a proper power up sequence for the display refer to the user manual of the used CPU module. The procedure may vary, depending on the used CPU module, also the handling of the LCD controller.

6.6 LCD 2 /GPIO interface on Baseboard

LCD 2 configuration:

The second LCD interface can be used as LCD2 or GPIO interface. In LCD2 configuration the example schematic is very similar to the circuit of LCD1 interface with the difference that only a 16-Bit Bus is available on the EXM connector.

To connect an 18-bit interface to the LCD 2 interface consult the following table.

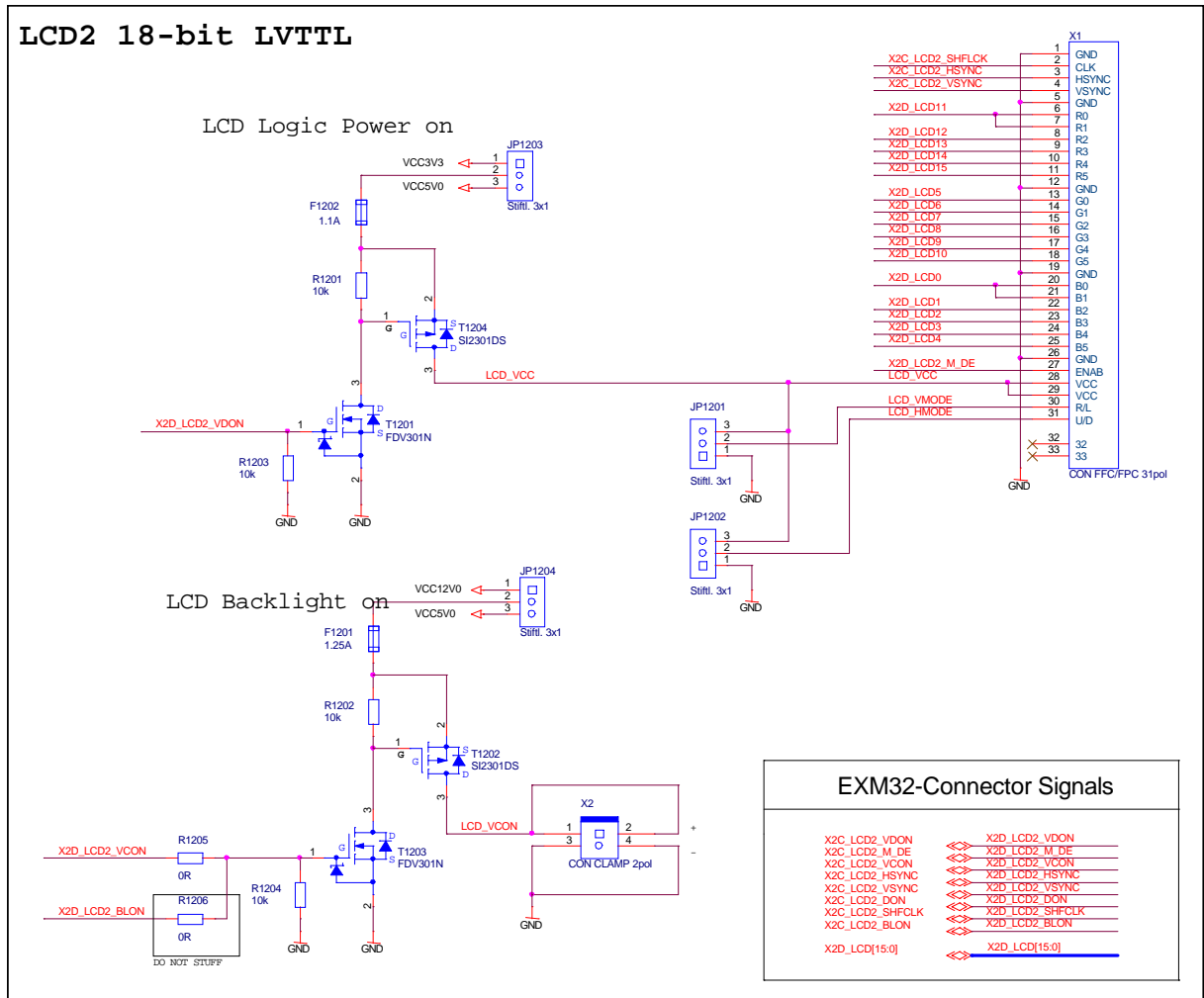


Figure 14 example schematic of a LCD2/GPIO-Interface on the baseboard in LCD2 configuration

SW Issues:

The handling of the LCD2 interface depends on the used CPU module. Refer to the according datasheet of the CPU module.

GPIO configuration

The GPIO interface can be directly connected to a arbitrary connector on the baseboard.

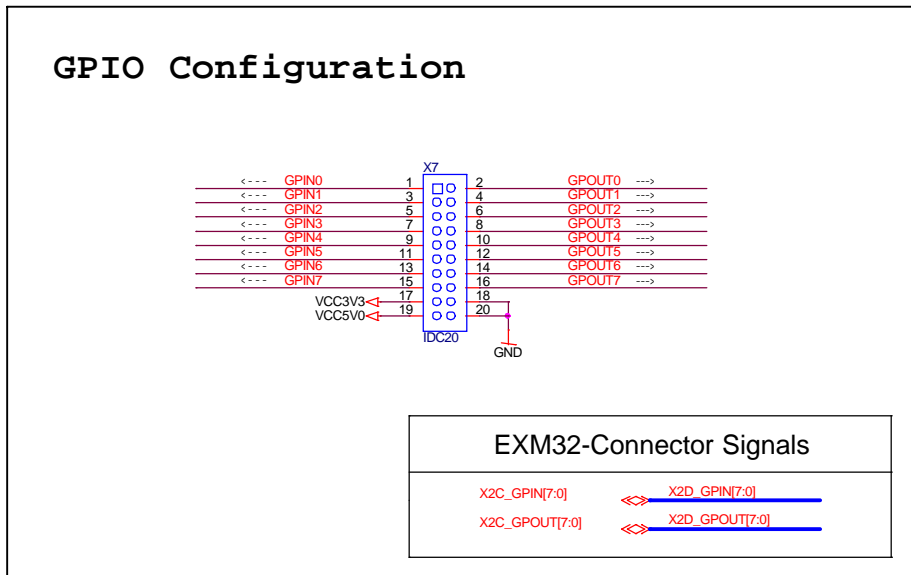


Figure 15 example schematic of an unbuffered LCD2/GPIO-Interface

If more driver performance or 3-stateable outputs are needed an external bus buffer on the baseboard is necessary. A external bus buffer is also needed if GPIO or LCD interface can be selected by logic.

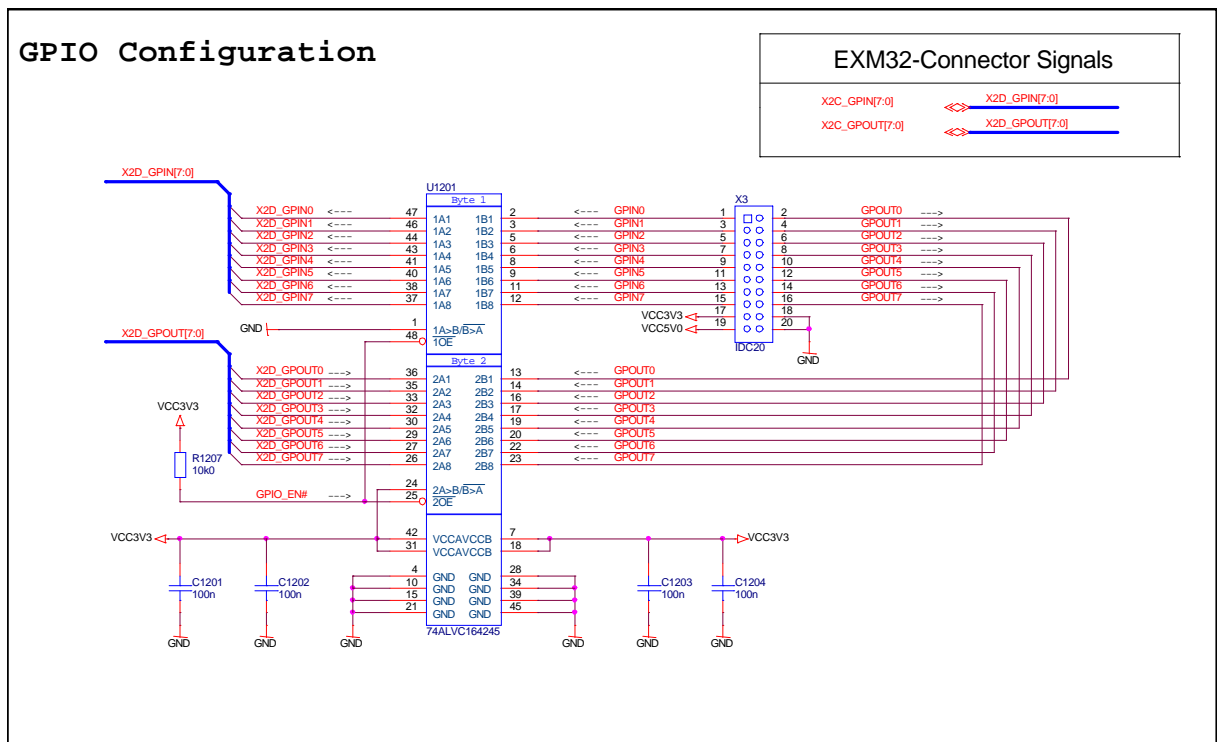


Figure 16 example schematic of a buffered LCD2/GPIO-Interface

6.7 Digital Audio (AC97, I2S) Interface on Baseboard

A digital audio interface is available on the EXM32 connector X1. The audio interface can be configured in AC97, I2S, Left Justified or Right Justified mode depending on the used CPU module. The digital audio signals have for AC97 and I2S dual functions the table beneath show the different signal routing dual function pins on the EXM connector for the AC97 and I2S mode.

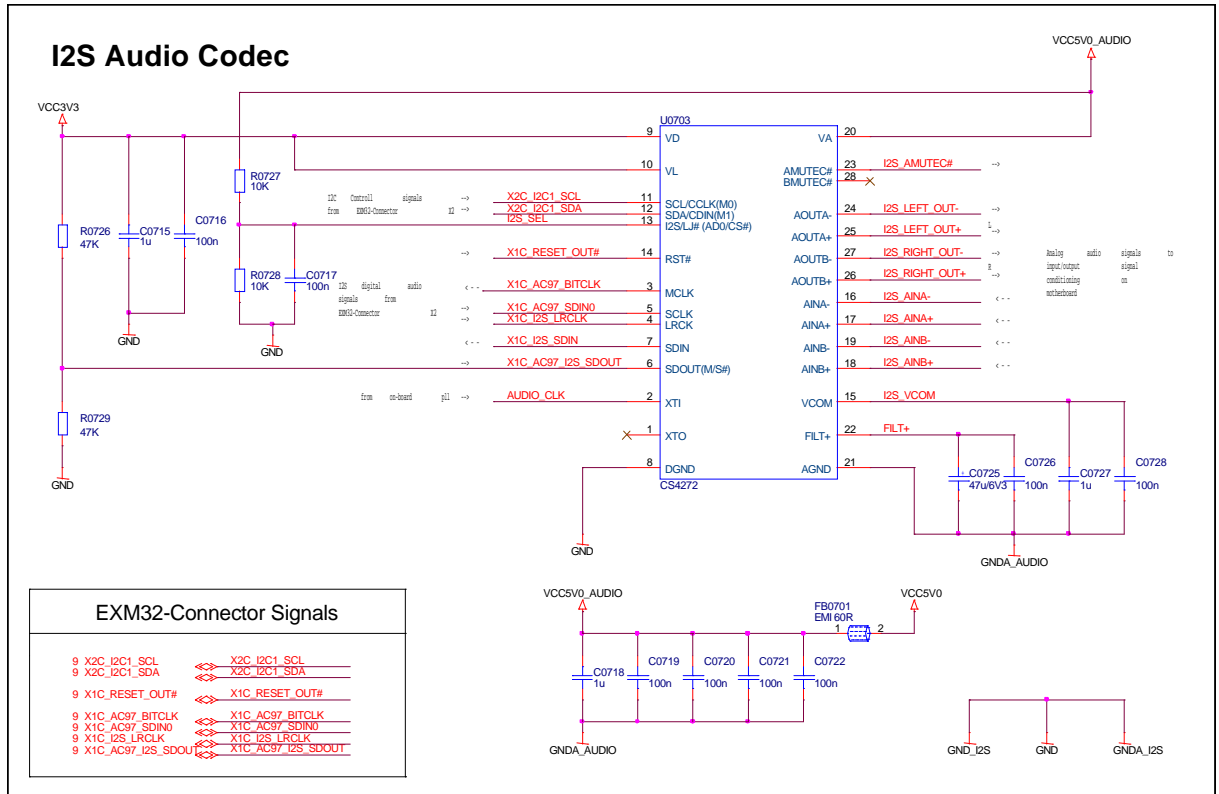


Figure 17 example schematic of an I2S codec implementation

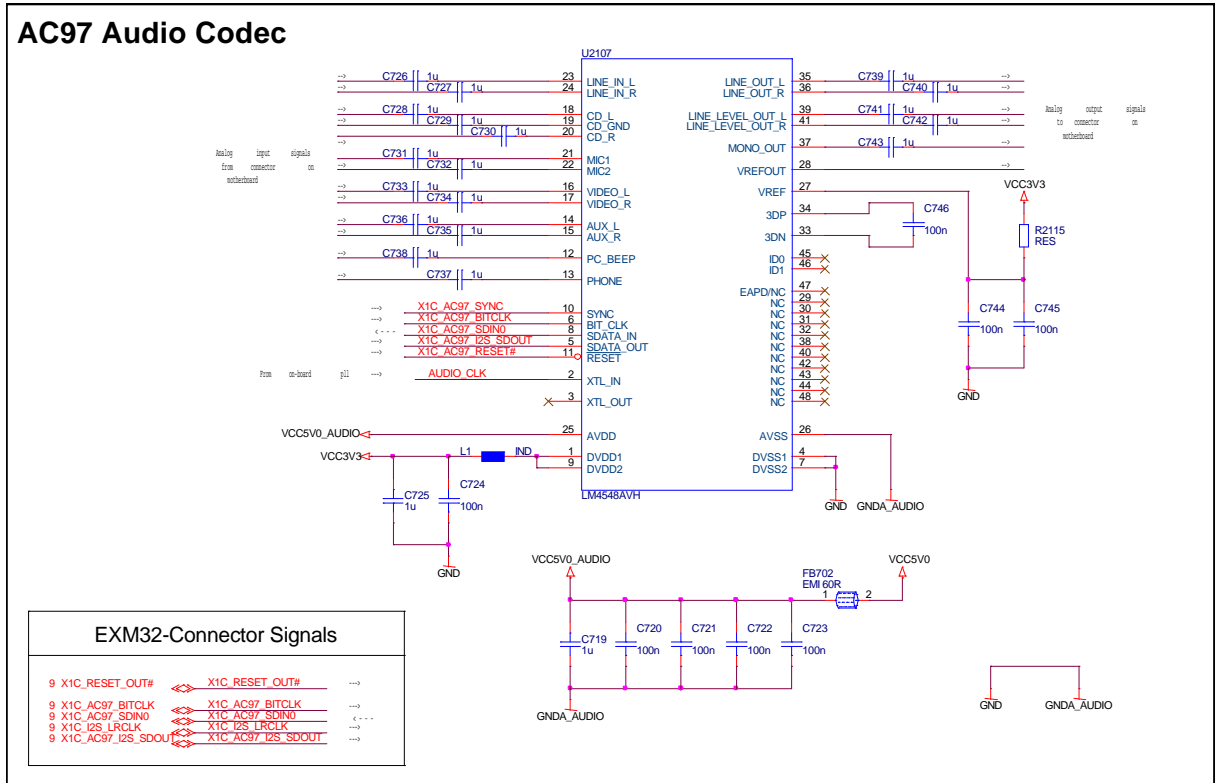


Figure 18 example schematic of an AC'97 codec implementation

SW Issues:

For the handling of the audio codec on the CPU module refer to the CPU datasheet and the CPU module user manual.

6.8 MMC/SD/SDIO Interface on Baseboard

A MMC/SD/SDIO interface is available on the EXM32 connector. If the interface is supported depends on the used CPU module. Refer to the CPU datasheet and the CPU module user manual.

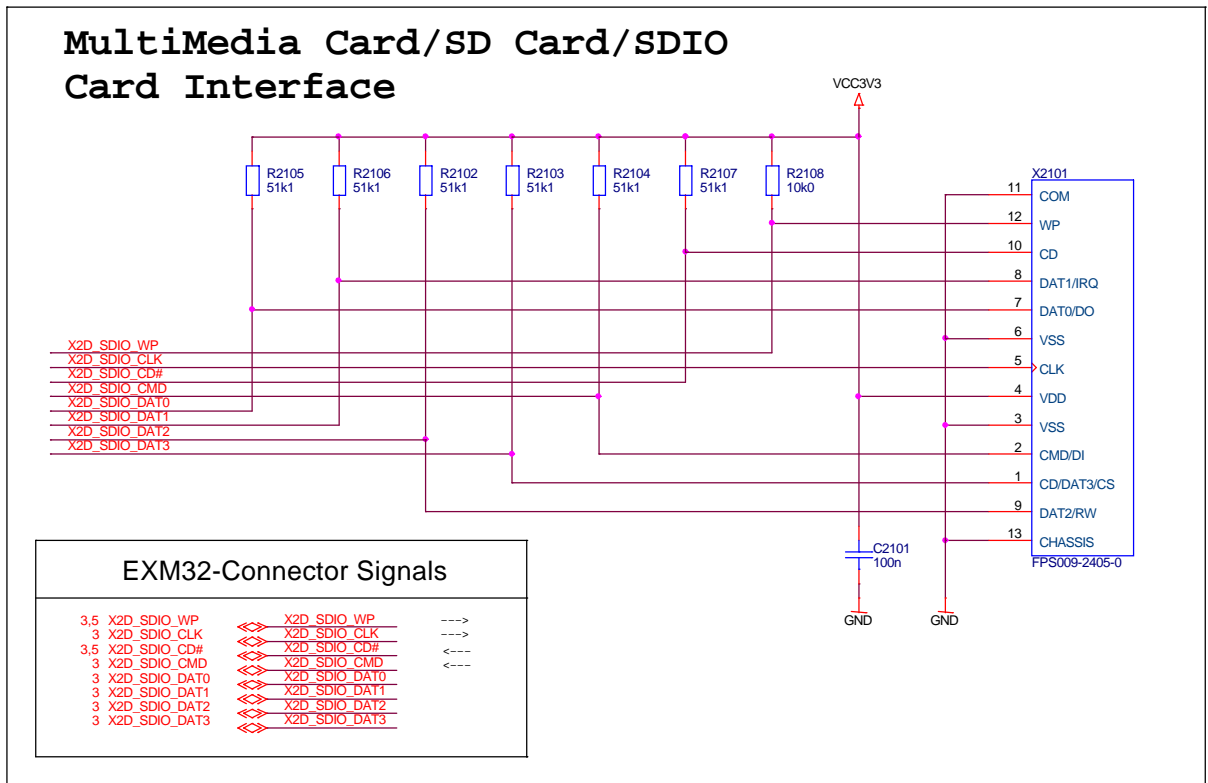


Figure 19 example schematic of a MMC/SC/SDIO interface implementation

6.9 CompactFlash Interface on Baseboard

A Compact Flash interface is available on the EXM32 connector. Refer to the CPU module user's manual, datasheet and the CompactFlash specification. It is possible to access two CompactFlash, PCMCIA sockets or two IDE devices with this interface.

The example schematic is only responsive to a CompactFlash implementation. All CompactFlash signals must be passed through transceivers on the baseboard to the Compact Flash connectors. This is necessary to make it possible to remove the CF card or put the card in while the system is running. The enable and direction signals for the buffers have to be generated by external logic on the baseboard. The logic equations for the signals are:

Buffer Enable:

$$CF_EN\# = \overline{(CF_CD1\#\vee CF_CD2\#)} \wedge (CF_SCKSEL) \wedge (CF_CE1\#\wedge CF_CE2\#)$$

Buffer direction :

$$CF_DDIR = \overline{X1B_R/W\#}$$

The example schematic only shows a CompactFlash interface implementation for PIO-mode. Serial resistors of 220ohm are recommended for all CF signals. For the following CF control signals pull up resistors are absolute necessary to guarantee a proper power up/reset sequence:

- CF_R_CE1#
- CF_R_CE2#
- CF_R_OE#
- CF_R_REG#
- CF_R_IOS16#
- CF0_CD1#
- CF0_CD2#
- CF0_R_RESET
- X1A_CF_WAIT#
- X1A_CF0_RDY_IRQ#
- CF_R_IOWR#
- CF_R_IORD#

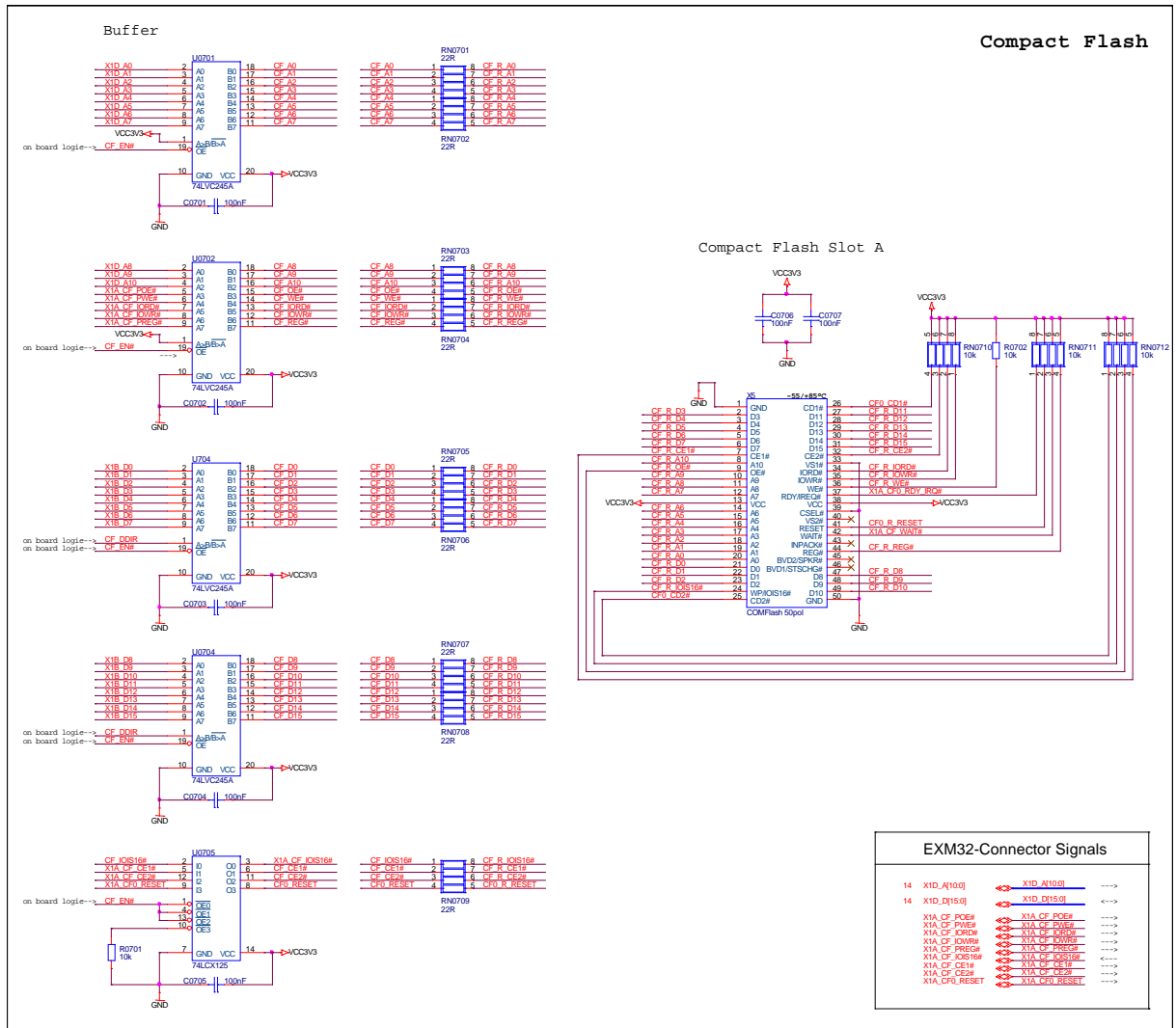


Figure 20 example schematic of a CompactFlash interface

6.10 Ethernet Interface on Baseboard

Ethernet signals are available on the EXM32 connector and can be connected to a RJ45 Ethernet connector via an Ethernet transformer. A recommended transformer type is HX1188NL (Pulse).

Transmission and receive lines have to be routed as differential pairs on the baseboard.

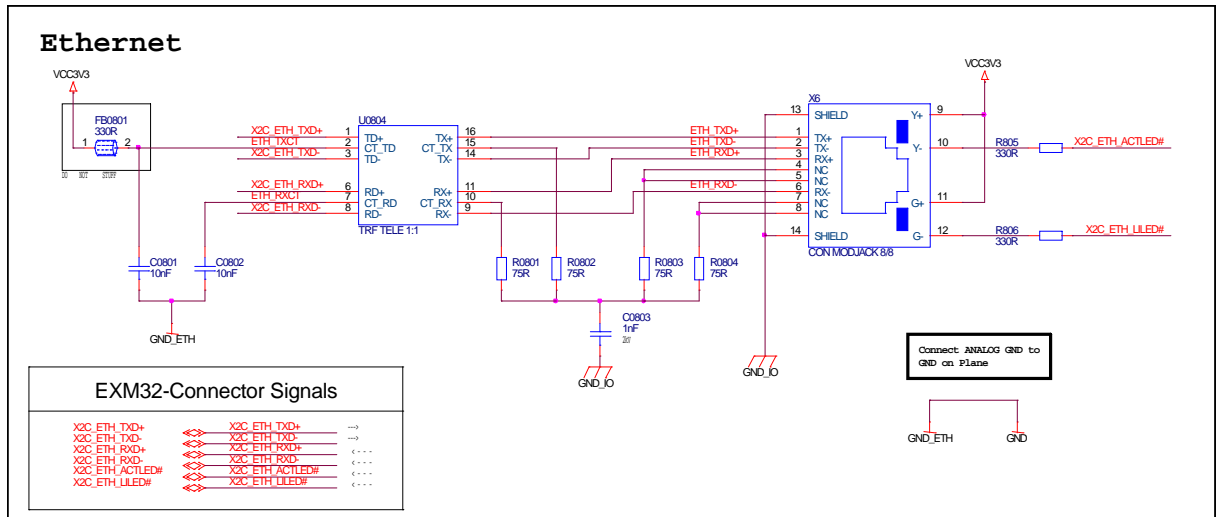


Figure 21 example schematic of an 10/100 Mbit Ethernet interface

6.11 Power Supply

An EXM32 module has got a maximum of 4 power connections:

a) VCC3V3

VCC3V3 is the main power supply for a CPU module and may carry up to 8A for the whole EXM32 module stack. All internal voltages on the module are derived from VCC3V3 and it is constantly monitored causing a RESET when outside of the 3,0-3,6V range.

b) VCC3V3STB

VCC3V3STB is a standby power-supply voltage which can be used to keep the SDRAM on the module alive in self-refresh mode while VCC3V3 is switched off on the baseboard ("suspend to RAM"), enabling the module to return from sleep-mode to full function in a very short time, provided the operating system image and the bootloader are designed to support this.

c) VBAT

VBAT is supposed to be a Lithium / button-cell type battery power supply used to power the RTC on the module. It's diode or'ed with VCC3V3STB on the module so while VCC3V3STB is active more or less no current is drawn from the battery.

d) VCC5V0

VCC5V0 is an auxiliary power supply mainly for expansion modules like the EXM32 Navigation Module where the GSM device requires voltages above 3,3V. If an EXM32 module does not make use of VCC5V0 it does not monitor it, so a 5V supply must only be provided if at least one EXM32 Module in the stack explicitly requires it.

6.12 ESD

Generally ESD-protection needs to be implemented on the baseboard as required for the custom application. Every connector pin or conductive part of the board which is accessible from outside of the enclosure with an ESD generator must protected using appropriate ESD components as close to the possible point of impact as possible which drain off the high-voltage spikes on a physically separate very low impedance path to GND.

End of Document